Comparison of Filter Components of Back-to-Back and Matrix Converter by Analytical Estimation of Ripple Quantities

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***Abstract*—This paper presents an analysis and comprehensive comparison between the passive filter component requirements of a matrix converter and a DC-link based back-to-back converter. Proper design of the filter components requires the estimation of the switching frequency components present in various voltages and currents. An accurate estimation of different ripple quantities is presented by simple analytical expressions and verified by MATLAB/Simulink simulations. The filters are designed and a quantitative comparison of the passive components is done.**

***Index Terms*—Matrix converter (MC), Back-to-back converter (B-BC), total harmonic distortion (THD)**

I. INTRODUCTION

AC-AC power electronic converters are being widely used in industry for applications like adjustable speed drives. Lately the matrix converter has emerged as a viable solution due to its unique properties like bidirectional power flow, open loop input power factor correction and minimum energy storage requirements resulting in a compact size [1]. However currently most of the applications primarily use the conventional voltage-source based back-to-back connected converters for some of their added benefits like voltage boosting capability and ease of use. Over the past decade, researchers have been comparing these two converters on various scales like performance, reliability issues, power losses, semiconductor area, passive component requirements, size and volume for different applications. Comparison based on the reliability issues due to voltage stress of the switches is presented in [2] for aerospace applications. A performance comparison of the two converters shows that matrix converters could be more tangible at high power, high voltage applications [3]. A comparative study of the two was done under open-circuit faults in the power switches [4] looking at the input/output currents THD and motor torque oscillations. A comparison to determine the highest output power based on the thermal stress of the switches is conducted, where it is shown that matrix converters perform better at low output frequencies [5]. A more detailed comparison based on semiconductor power losses is done in [6]–[8]. However with advancing technology and emerging power semiconductor devices, device stress and losses might not be the dominating factor. A very important aspect is the volume of the passive components [9].

This paper compares the filter requirements of the matrix converter with a back-to-back converter based on analytical estimation of the ripple quantities. The MC injects harmonic currents and a B-BC produces switched voltages at its input. An input LC filter of the matrix converter is designed and compared with an LCL filter and DC-link capacitor of the back-to-back converter. Use of an LCL filter reduces the inductor size and provides better attenuation of higher order harmonics in the grid current. Most of the design approaches previously considered that the ripple quantities have been obtained from a simulation model [6], [10]. Others design it by approximating the switching ripple to be equal to the fundamental component [11]. Analytical estimation of MC input ripple current [12] and B-BC input harmonic voltages [13] [14] are derived using much complicated Bessel functions. The authors in [15] analyze the THD in the inverter side inductor of the B-BC for the LCL filter design. Different other design procedures have been presented for the input LCL filter design of front end rectifiers or grid connected inverters [16]–[18] and matrix converters [19]–[21]. Analytical calculation of current stress on the DC-link considering the front end to be a diode bridge is given in [22]. The analytical approach to estimate the input current ripple for the matrix converter has been presented in [23].

This paper derives simple analytical expressions for the ripple quantities in a back-to-back converter as well, from the modulation strategy as a function of the modulation indices and load power factor. The converters are then modeled for both fundamental and switching frequency components. The two models are considered independently by principle of superposition and design equations are derived to calculate the filter parameters. The designed filters of both the converters are compared. Section II and III describe the modulation strategy, control and modeling of the two converters for filter design. In section IV the passive components design is explained in detail, followed by Simulation, Comparison and Conclusion in Section V, VI and VII respectively.

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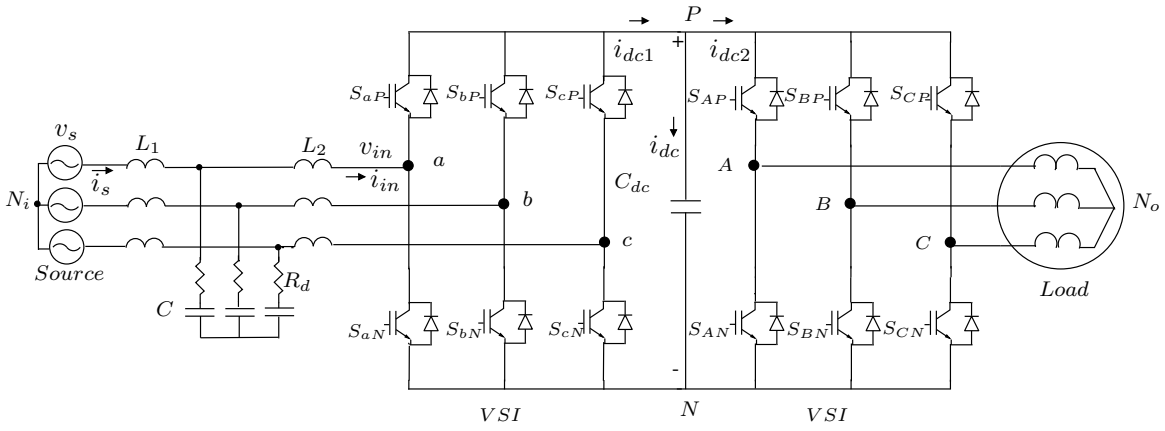
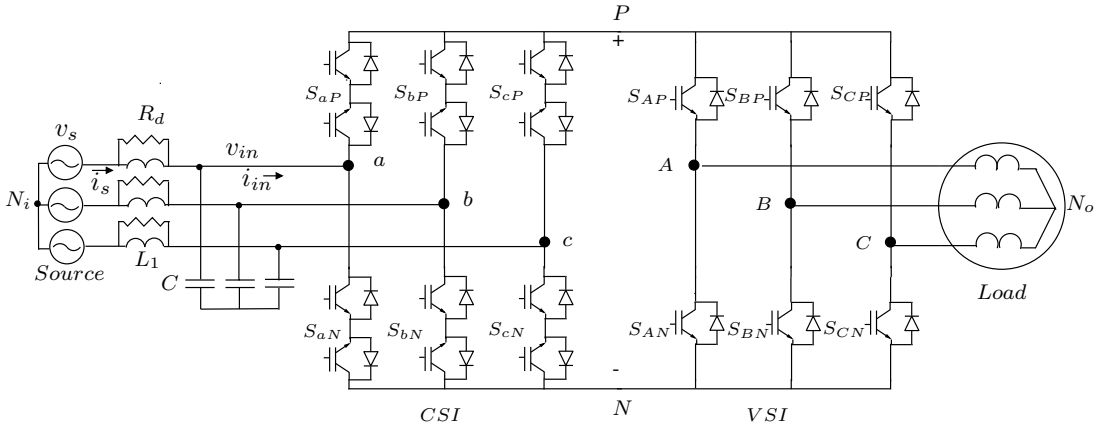


(a)



(b)

Fig. 1: (a) Back-to-back Converter, (b) Matrix Converter

II. ANALYSIS: BACK-TO-BACK CONVERTER

A. Modulation and Control

The back-to-back converter is composed of two voltage source inverters (VSI) connected in a back to back fashion with a DC-link capacitor as shown in Fig. 1(a). Each converter acts as an independent VSI and is modulated using the six active voltage space vectors as shown in Fig. 3(b). Considering the front end VSI, the reference voltage vector v_{ref} is generated from two adjacent active vectors and zero vector whose duty ratios are given by (1) where m_{V1} is the ratio of peak of the fundamental component of the input voltage to the DC-link voltage V_{dc} and α is the angle between the first vector and v_{ref}. The DC-link voltage is maintained constant with a closed loop control, [24]. An outer voltage loop regulates the DC-link voltage (V_{dc}) and two inner current loops control the real and reactive power flow. By just transferring real power demanded by the load, unity power factor is maintained at the grid.

$$\begin{aligned} dV_{11} &= \sqrt{3} m_{V1} \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_{21} &= \sqrt{3} m_{V1} \sin\alpha \end{aligned} \tag{1}$$

B. Modeling of back-to-back converter for filter design

The modulation of the back-to-back converter generates switched voltages at its input v_{in}. The instantaneous input phase voltage referred to grid neutral can be expressed in terms of three instantaneous phase voltages referred to the negative DC-link (2). Fig. 2 shows three input phase to negative DC-link voltages and one input phase a to neutral voltage v_{aN_i}. Considering conventional space vector pulse width modulation, over one sampling cycle in the first sector, the instantaneous input line to neutral voltage is composed of levels $2V_{dc}/3$ and $V_{dc}/3$ as shown in Fig. 2. Hence the square RMS of input line to neutral voltage over one sampling cycle in the first sector is given by (3). Now the square RMS of input voltage over the first sector is found by averaging out (3) over first sector as shown in (4). The

expressions are similarly obtained for second and third sectors. This computation repeats for the remaining sectors. Assuming the DC-link voltage is constant, the input RMS voltage over one fundamental cycle is found from the RMS of each sector (5) as a function of just the modulation index m_{V1} of the front end converter (6). The ripple voltage needed for filter design is obtained by subtracting the fundamental component of input voltage from total RMS voltage.

$$v_{aN_i} = \frac{1}{3}(2v_{aN} - v_{bN} - v_{cN}) \tag{2}$$

$$v^2_{aN_{iRMS,T_S}} = dV_{11}\left(\frac{2V_{dc}}{3}\right)^2 + dV_{12}\left(\frac{V_{dc}}{3}\right)^2 \tag{3}$$

$$V^2_{aN_iRMS_{SECTOR}} = \frac{1}{\pi/3}\int_{SECTOR} v^2_{aN_{iRMS,T_S}} d(\omega_i t) \tag{4}$$

$$V^2_{aN_iRMS} = \frac{1}{3}\sum_{i=1,2,3} V^2_{aN_iRMS_{SECTORi}} \tag{5}$$

$$V^2_{aN_iRMS} = \frac{2\sqrt{3}m_{V1}}{3\pi}V^2_{dc} \tag{6}$$

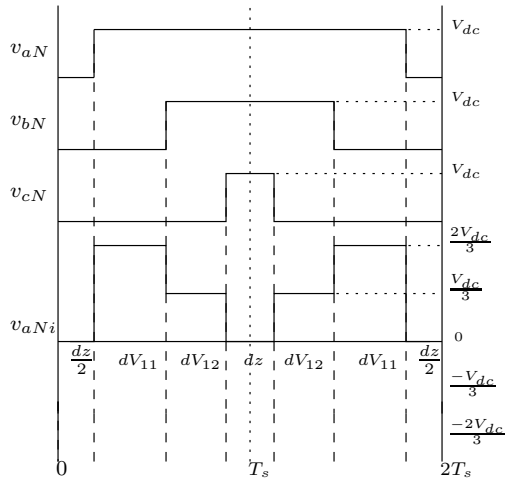


Fig. 2: Instantaneous input line to neutral voltage generation in first sector from line to negative DC-link voltages

C. Current stress on DC-link

For a suitable design of the DC-link capacitor, the current ripple passing through it is analytically computed. The instantaneous current flowing into the capacitor is the difference of the two DC-link currents generated because of the switching of the two VSI's. Hence the square RMS of the capacitor current is as shown in (7). Considering just the output converter, the instantaneous DC-link current $i_{dc1} = i_A$ during time interval $dV_{21}T_s$ and $i_{dc1} = -i_C$ during time interval $dV_{22}T_s$ in the first sector (8). The RMS current obtained by considering just the first sector remains same in the other sectors. The RMS current expression due to switching of the input side converter is similar. Next the total average value of the remaining part $2I_{dc1}I_{dc2}$ is computed in a similar way. The instantaneous value in the first sector is as shown in (9). Three different expressions are obtained for the first three sectors which repeat for the other three sectors. Hence the net RMS current flowing through the capacitor is as shown in (10).

$$I^2_{dc,RMS} = I^2_{dc1,RMS} + I^2_{dc2,RMS} - 2\int_0^{T_s} I_{dc1}I_{dc2} \tag{7}$$

$$i^2_{dc2_{RMS,Ts}} = dV_{21}(i_A)^2 + dV_{22}(-i_C)^2 \tag{8}$$

$$i_{dc1,Ts}i_{dc2,Ts} = \{dV_{11}(i_a)+dV_{12}(-i_c)\}\{dV_{21}(i_A)+dV_{22}(-i_C)\} \tag{9}$$

$$I^2_{dc_{RMS}} = \frac{5\sqrt{3}}{2\pi}m_{V1}I^2_{in} + \frac{\sqrt{3}}{\pi}m_{V2}I^2_o\left(2cos^2\phi_o + \frac{1}{2}\right) - \frac{9}{2}I_{in}I_o m_{V1}m_{V2}cos\phi_o \tag{10}$$

III. ANALYSIS : MATRIX CONVERTER

A. Indirect Modulation of Matrix Converter

Space vector modulation (SVM) results in the highest voltage gain in a matrix converter and is hence considered in this paper. Indirect modulation [25] of matrix converter is the most conventionally used SVM and can be described using two fictitious converters acting as a current source inverter (CSI) and a voltage source inverter (VSI) connected through a virtual DC-link as shown in Fig. 1(b). This topology is also referred to as the indirect matrix converter topology. The CSI employs six active current space vectors as shown in Fig. 3(a). Similarly Fig. 3(b) shows the six active voltage space vectors of the VSI. In total, the indirect modulation makes use of eighteen active vectors of both the converters. The duty ratio of two adjacent space vectors of the CSI are given by (11), where m_I is the ratio of peak of the fundamental component of the input current to the virtual DC-link current. The switching sequence applied over a cycle is given in Fig. 3(c). Combining the switching sequence of the two converters, the actual switching signals can be obtained for a conventional direct matrix converter also.

$$\begin{aligned} dI_1 &= m_I \sin\left(\frac{\pi}{3} - \beta\right) \\ dI_2 &= m_I \sin\beta \end{aligned} \tag{11}$$

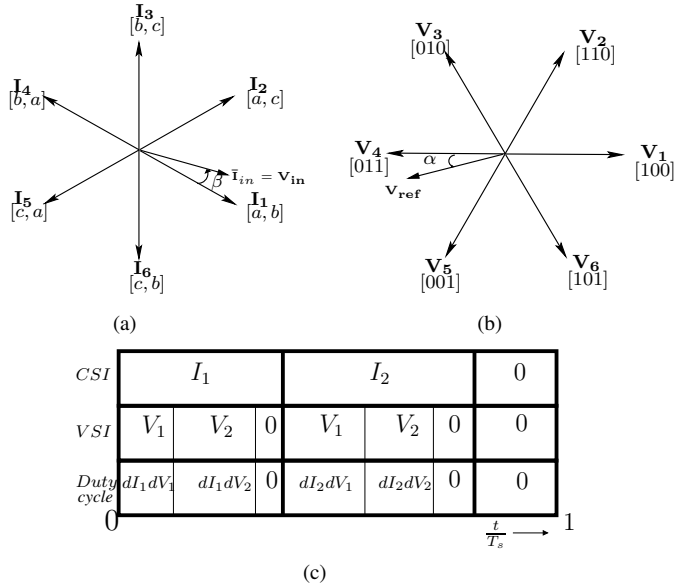


Fig. 3: (a) Current space vectors produced by CSI, (b) Voltage space vectors produced by VSI, (c) Switching sequence of Matrix converter

B. Modeling of Matrix Converter for Filter design

The matrix converter is modeled as a current source (per-phase) both for the fundamental and the higher harmonic components (multiples of switching frequency). For the fundamental component of the input frequency, the matrix converter can be modeled as a resistive load R_e when modulation ensures input power factor correction, in terms of the output load impedance ($|Z_L| = \frac{V_o}{I_o}$) as shown in (12).

$$R_e = \frac{V_{in}}{I_{in}} = \frac{Z_L}{(\frac{3}{2})^2 (m_I m_V)^2 \cos\phi_o} \tag{12}$$

For the switching frequency component, the input RMS current ripple is analytically estimated as explained in [23]. The input current over one sampling cycle is composed of different output currents over time periods $dI_1dV_1T_s$, $dI_1dV_2T_s$, $dI_2dV_1T_s$ and $dI_2dV_2T_s$ as shown in Fig. 3(c). During time period $dI_2dV_1T_s$, $i_a = i_B + i_C = -i_A$ and during $dI_2dV_2T_s$ period, $i_a = i_C$ as shown in Fig. 4(a) and Fig. 4(b). This is assuming that input current and output reference voltage average vectors are as positioned in Fig. 3(a) and Fig. 3(b). Similarly by considering the time intervals $dI_1dV_1T_s$ and $dI_1dV_2T_s$ it is possible to obtain the expressions for the square RMS of the input line current i_a over a sampling cycle (13). The total input RMS current is obtained as a function of load power factor $cos\phi_o$ and modulation index $m_I m_V$ of the matrix converter as shown in (14).

$$\begin{aligned} i^2_{a_{RMS,Ts}} &= (dV_1dI_1 + dV_1dI_2)(-i_A)^2 \\ &\quad +(dV_2dI_1 + dV_2dI_2)(i_C)^2 \end{aligned} \tag{13}$$

$$\begin{aligned} I^2_{a_{RMS}} &= \frac{3\sqrt{3}m_I m_V I_o^2}{\pi^2}\left(\frac{\pi\sqrt{3}}{12} + \frac{3}{8}\right)(1+\cos 2\phi_o) \\ &\quad +\frac{3\sqrt{3}m_I m_V I_o^2}{\pi^2}\left(\frac{\pi}{12} - \frac{\sqrt{3}}{16}\right)\sin 2\phi_o \end{aligned} \tag{14}$$

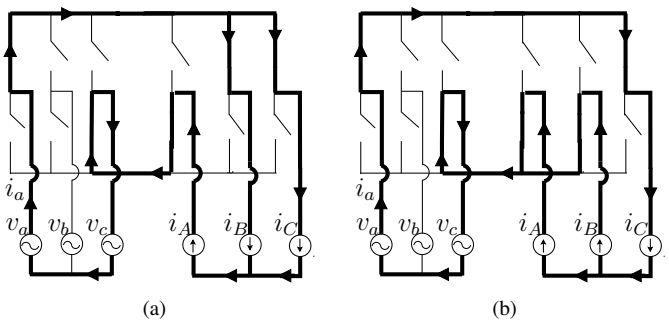


Fig. 4: Current flow paths for time periods (a) $dI_2dV_1T_s$, (b) $dI_2dV_2T_s$

IV. PASSIVE COMPONENTS DESIGN

A. Input filter design of Back-to-Back Converter

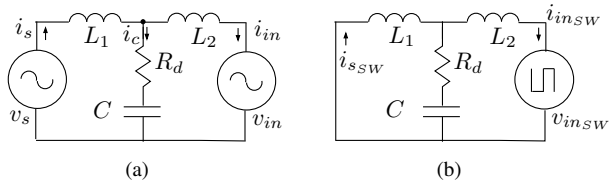


Fig. 5: Per-phase equivalent circuit of back-to-back converter input filter at (a) fundamental frequency and (b) switching frequency

The back-to-back converter generates switched voltages at its input which flow a distorted current. The allowable THD in the input current of the B-BC converter generally lies between $10-30\%$ depending on the grid impedance limits. A basic L filter alone becomes huge and is not sufficient to limit the grid current THD to a minimum. Hence an LCL filter is generally used to limit the grid side current ripple within 5% according to IEEE standards. The LCL filter is modeled for both fundamental (Fig. 5(a)) and switching frequency (Fig. 5(b)). For the ripple component, the B-BC is modeled as a switching voltage source whose RMS is calculated before. The harmonic components occur at multiples of switching frequency due to pulse width modulation. As the dominant harmonics occur at the switching frequency $1/T_s$, from the filter design perspective it is assumed that all of the ripple energy is concentrated at the switching frequency. A damping resistor R_d is connected in series with the capacitor C to damp any oscillations occurring due to resonance

of the filter components. The ratio of input voltage ripple at the front end converter to the permitted input current ripple is given by the input impedance (15). The allowable grid current THD can be expressed as a function of converter input current THD (16). For the fundamental component, the converter is modeled as a sinusoidal voltage source V_{in}. With a larger capacitor, more reactive power flows into the capacitor raising the current rating of inductor L_2 and so of the switches. But the capacitor can not be very small either which will increase the inductor size required to meet the same attenuation requirements. Hence the current flowing through the capacitor (17) is restricted to be $5-15\%$ of source current. The power loss in the damping resistor (18) should not exceed 0.001% of the rated power P of the converter. Using the four equations, we can solve for $L1$, $L2$, C and R_d.

$$\frac{V_{in_{SWRMS}}}{I_{in_{SWRMS}}} = \left| j\omega_s L_2 + \frac{(j\omega_s L_1)\left(\frac{-j}{\omega_s C} + R_d\right)}{j\omega_s L_1 - \frac{j}{\omega_s C} + R_d} \right| \tag{15}$$

$$I_{s_{SWRMS}} = I_{in_{SWRMS}} \left| \frac{\frac{-j}{\omega_s C} + R_d}{\frac{-j}{\omega_s C} + R_d + j\omega_s L_1} \right| \tag{16}$$

$$I_{c_{RMS}} = \left| \frac{V_{s_{RMS}} - j\omega L_1 I_{s_{RMS}}}{\frac{-j}{\omega C} + R_d} \right| \tag{17}$$

$$\frac{P_{loss}}{P} = \frac{R_d I_{c_{RMS}}^2}{V_{s_{RMS}} I_{s_{RMS}}} \tag{18}$$

B. DC-link capacitor design of Back-to-back Converter

The switching of converters generate high frequency current harmonics at the DC-link. This current ripple as given by (10) should pass through the capacitor C_{dc} for normal operation of the converter. The DC-link capacitor is designed based on a minimum ripple on the DC-link voltage in order to maintain the modulation of both front and load end inverters, and can be calculated using expression (19). The DC-link capacitor value also depends on output torque ripple variations, unbalance issues and ride-through capability, but they are not considered in this design.

$$\frac{V_{dc_{ripple}}}{I_{dc_{RMS}}} = \frac{1}{\omega_s C_{dc}} \tag{19}$$

C. Input filter design of Matrix Converter

A single stage input LC filter is designed as explained in [23], to provide attenuation of the ripple in the grid current. Analyzing circuit at switching frequency as shown in Fig. 6(b) it is possible to express the allowable ripple in converter voltage $V_{in_{SWRMS}}$ and grid current $I_{s_{SWRMS}}$ in terms of $I_{in_{SWRMS}}$

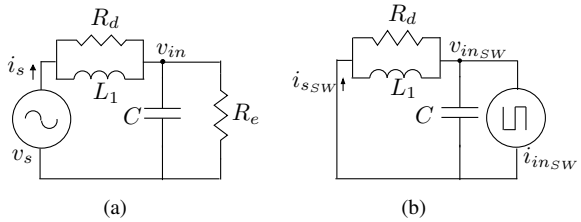


Fig. 6: Per-phase equivalent circuit of matrix converter input filter at (a) fundamental frequency and (b) switching frequency

(20), (21). Analyzing the circuit for the fundamental component Fig. 6(a), it is possible to compute the ratio of the power loss in the damping resistor to the total output power of the converter (22). For a given THD in the grid current, RMS ripple of the converter voltage and percentage loss in the damping resistor, (20), (21) and (22) can be solved simultaneously to determine L, C and R_d.

$$V_{in_{SWRMS}} = \frac{I_{in_{SWRMS}}}{\sqrt{(\omega_s C - \frac{1}{\omega_s L_1})^2 + \frac{1}{R_d^2}}} \tag{20}$$

$$I_{s_{SWRMS}} = \frac{I_{in_{SWRMS}}}{\sqrt{1 + \frac{(1-\omega_s^2 L_1 C)^2 - 1}{\left(1 + \frac{\omega_s^2 L_1^2}{R_d^2}\right)}}} \tag{21}$$

$$\frac{P_{loss}}{P} = \frac{I_{s_{RMS}}}{V_{s_{RMS}}} \left(\frac{\omega^2 L_1^2 R_d}{\omega^2 L_1^2 + R_d^2}\right) \tag{22}$$

V. SIMULATION

The two power electronic converters as shown in Fig. 1(b) and Fig. 1(a) are simulated with ideal switches in MATLAB/Simulink for an industrial drive of 20 kW, 480 $V_{(LL-RMS)}$. The drive runs a three phase R-L load of 0.8 power factor at a switching frequency of 10 kHz. The DC-link voltage of the back-to-back converter is maintained at 750 V with closed loop control. The modulation indices of both the converters are adjusted to generate same currents at the output for a proper comparison. Different input and output frequencies of 60Hz and 30Hz respectively were selected to show that the analytical expressions obtained at different input-output frequencies remains unchanged as explained in Section II and III. The maximum allowable grid current ripple is assumed to be 2%. For the back-to-back converter the THD level in the input current of the front end inverter is assumed to be 15% and the maximum reactive power drawn by the capacitor is limited to 5% of rated values. The voltage ripple in the DC-link voltage is limited to 1% to allow constant DC-link voltage. Fig. 7(a) shows the input voltage, input current and their filtered waveforms for the matrix converter. Frequency spectrum of various voltage and current waveforms are plotted in Fig. 8(a). For MC, from these

two figures, it is evident that the voltage drop across the filter is negligibly small and there is almost unity power factor. Similar results are shown for the back-to-back converter in Fig. 7(b) and Fig. 8(b). The DC-link voltage and currents for the back-to-back converter are shown in Fig. 7(c). The RMS values obtained from simulation closely match the analytical calculations as described in Section II and III which verifies the analysis.

VI. COMPARISON

The designed values of the passive components are shown in Table I. As can be seen, the grid side inductor L_1 of matrix converter is nearly 1.6 times larger in magnitude than that of the back-to-back converter. However, there is an additional large boost inductor L_2 present in the back-to-back converter. Thus the combined inductance needed on the input side is three times larger for a B-BC than a MC. Both the converters see the same fundamental component of the input line currents and hence volume of the inductors scale directly according to the magnitude of inductance (volume $\propto LI^2$). However, the boost reactor of the B-BC has large iron loss due to high frequency components in the input current. In contrast, the input reactor of the MC experiences just the fundamental current as most of the high frequency ripple current flows through the filter capacitor. Hence it has small iron loss. The filter capacitance C of matrix converter is 3.6 times larger in magnitude as compared to that of back-to-back converter. Both the capacitors are subject to same voltage stress. Also, the losses incurred which affect the overall lifetime also depend on the ripple current flowing through the capacitors. The matrix converter input filter is subject to much higher current stress as compared to the back-to-back converter. The RMS current flowing through the capacitors (3.2 A) in B-BC is composed of some reactive current and remaining ripple current. Whereas the MC filter capacitors see a much larger current ripple (20.5 A) as analytically calculated in Section III. So in a nutshell, the MC capacitors have 3.6 times the magnitude than that of B-BC and are also subject to 10 times higher current stress which reduces its overall lifetime. The back-to-back converter also has a DC-link capacitance of 53.06 μF which is subject to a current stress (24.5 A) as analytically calculated in Section II and an applied voltage of 750V. This unreliable DC capacitor, which is usually electrolytic is absent in case of a matrix converter.

TABLE I: Comparison: filter components

Parameters	MC	B-BC
$L_1(\mu H)$	310.25	187.01
$L_2(\mu H)$	-	799.33
$C_1(\mu F)$	41.61	11.51
$C_{dc}(\mu F)$	-	53.06

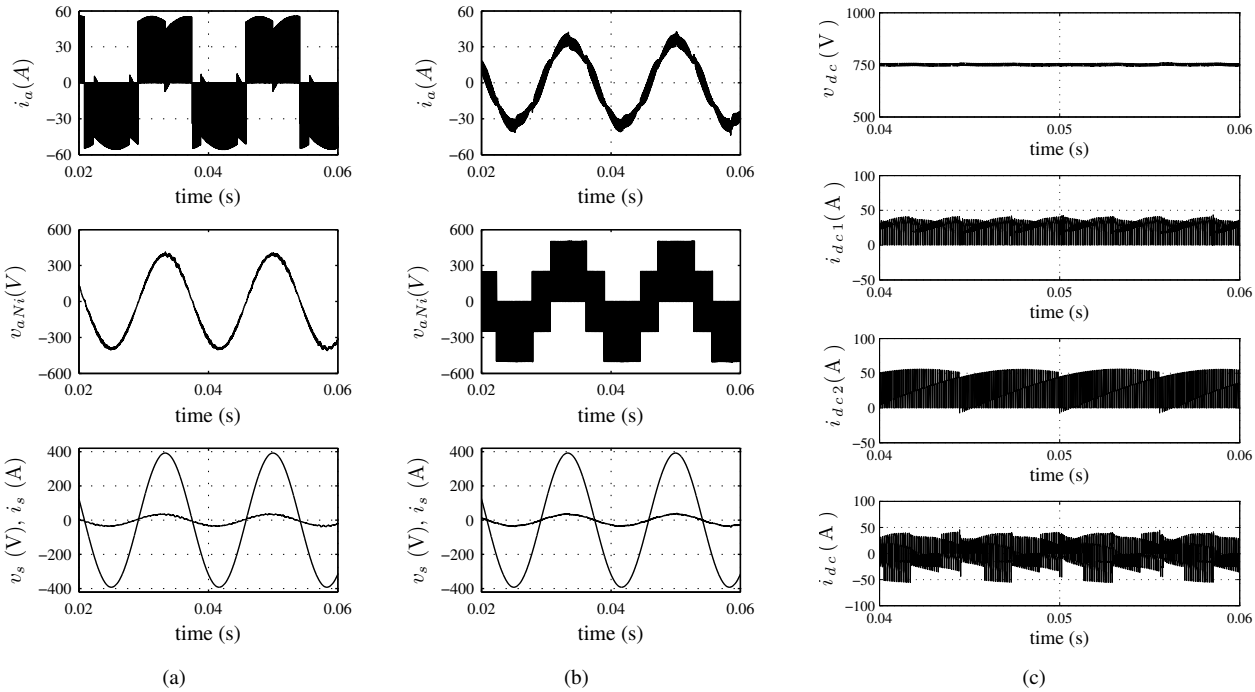


Fig. 7: Input current (top), input voltage (middle) and filtered grid current and voltage (bottom) of (a) Matrix converter and (b) Back-to-back converter. (c) DC-link voltage v_{dc} (top), DC-link current from front end converter i_{dc1} (second from top), DC-link current from load side converter i_{dc2} (third from top) and total current through capacitor i_{dc} (bottom) of Back-to-back converter

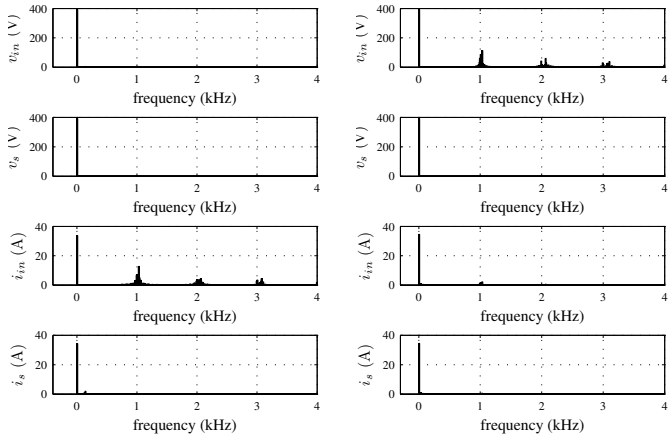


Fig. 8: Frequency spectrum: (a) Matrix converter, (b) Back-to-back converter

VII. CONCLUSION

A design procedure to determine the filter components for a matrix converter and back-to-back is presented using analytical estimation of ripple quantities. The computation is independent of any cumbersome fourier analysis and depends only on the modulation index and load power factor. This eliminates the need for a simulation model and the filter components can be designed from simple mathematical expressions. The designed filter results in high quality grid current, near unity power factor, negligible drop across filter and minimum loss in damping resistor. A quantitative comparison is presented between the reactive elements of both the converters.

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